Black Sea Economic Cooperation

Project cipher **BSEC/PDF/13/05 2007**

Network of Integrated Circuit Design Teaching Centers in Black Sea Region

Final Report

Niš, Yerevan, Sofia

June 2008

Contents

Executive Summary

Project entitled "Network of Integrated Circuit Design Teaching Centers in Black Sea Region" (NICDTC) initiated establishing mutually compatible knowledge and skills of integrated circuits design engineers in BSEC countries. We expect to strength competitiveness of NICDTC members with other European regions in the field of Information Communication Technologies. The Project Partners comes from three countries within BSEC Region:

1. Faculty of Electronic Engineering, University of Nis, Serbia
2. State Engineering University of Armenia (SEUA) "Microelectronic Circuits and Systems" Interdepartmental Chair (MCS), Yerevan, Armenia
3. Faculty of Electronics, Technical University of Sofia (TUS), Sofia, Bulgaria

The Project activities were performed in three phases. Namely

1. Preparing phase
2. Executive phase
3. Final phase

During the preparing phase all three design centers (nodes of the network) gave a comprehensive analysis of own current status and made a SWOT analysis of the network was made. As result, all partners have prepared recommendations for modifications in each node to harmonized syllabi. One meeting was held in Sozopol, Bulgaria in September 2007.

Throughout the executive phase all participants give effort to upgrade hardware and software resources, to modify syllabi and establish contact with other IC design centers in Europe and BSEC region. The most significant software upgrading possibilities come from benefits of EUROPRACTICE Service. The annual fees for EUROPRACTICE were covered by funds given by PDF. This helped a lot to all three nodes to approach to the same IC technology resources what is indispensable for further collaboration between design centers. As there was no money approved for hardware upgrading within this project, every participant had to provide it using other sources. A lot of work that is not clearly visible from the outside but is crucial for reaching the goal of the Project was done in syllabus harmonization. The only observable fact in this sense is the transformation from study scheme 3 + 2 (3 years for bachelor and 2 years for graduate studies) at Faculty of Electronic Engineering, University of Nis, Serbia to 4 + 1 in order to match with syllabi at TU Sofia and SEAUA Yerevan. It should be stressed again that much effort has been done in upgrading many courses in all three nodes.

Besides, during the project realization, all three participants had connections with experienced European Design Centers and other centers from BSEC Region. However due to the reduced approved funds these activities were supported from other sources.

The second meeting the participants had in Nis, Serbia in May 2008. The concluding meeting was planned for June 2008 during the ETRAN Conference held on Plaic Lake, Serbia.

The purpose of the final phase was to summarize the achievements of the project and to prepare participants for application for a European project.

The achievements of the Project are measured through the attainment of all three participants and are described in details in the Final Report. Here is the brief summary.

Common benefits

1. Each institution got thorough analysis of teaching possibilities in domain of IC Design in scope of syllabus, human resources, software resources and hardware resources.
2. The roadmap for future activities toward networking is defined
3. Connection with IC Design centers in more BSEC countries (re)established
4. Connection with IC Design centers in more EU countries (re)established
5. Student projects were exchanged
6. Agreement made about join application for future European projects

Benefits for particular participants are:

Serbian partner

- Syllabus completely rearranged
- Software tools resources considerably enlarged with Mentor Graphics design platform
- Paid Fee for EUROPRACTICE Service and Cadence Design Tool license

Armenian partner

- Syllabus updated
- Paid Fee for EUROPRACTICE Service

Bulgarian partner

- Syllabus updated
- Hardware upgraded
- Paid Fee for EUROPRACTICE Service and Cadence Design Tool license

1 Introduction

Project entitled "Network of Integrated Circuit Design Teaching Centers in Black Sea Region" (NICDTC) is aimed to initiate establishing mutually compatible knowledge and skills of integrated circuits design engineers in BSEC countries in order to strength competitiveness with other European regions in the field of Information Communication Technologies. The strategic gain of the project is establishing a method to slow-down or even to stop the brain-drain process from BSEC Region, as will be explained later on.

According to this goal the three educational institutions: Faculty of Electronic Engineering - University of Niš in Serbia; State Engineering University of Armenia "Microelectronic Circuits and Systems" Interdepartmental Chair (MCS) of Yerevan, Armenia and Faculty of Electronics, Technical University of Sofia (TUS), Sofia, Bulgaria defined objectives to

- Introduce European standards for education in the field of Integrated Circuit (IC) Design (having in mind the Bologna Declaration)
- Share the existing design resources in BSEC countries and
- Establish partnership with developed countries.

The work on this project opened opportunities for collaboration in other joint projects. Besides, the three institutions agreed to share already designed circuit cores in a form of intellectual property. Namely, all IC cores designed by any node of the network can be available to other partners under the best possible conditions. Therefore each node of the network becomes more competitive on the market. Consequently, chances to enter into international projects and opening of job possibilities for IC designers will arise.

The Network gives engineers chances to work in the field of high-tech industry in homeland with the possibility to exchange experiences with colleagues working in leading design centers.

As the NICDTC fits to Tempus project, Marie Curie Excellence Grants and other, the participants agree to apply for any of them as potential financial tool for the future. Looking for appropriate action within other projects of the 7th Framework program (like Research Training Networks, Early Stage Research Training and Transfer of Knowledge) where all participants will be able to contribute - is one of final goals of the project. Through this activity we expect to provide stabile funds for NICDTC in the future.

Activities of the project were planned and accomplished within

1) Preparing phase,
2) Executive phase and
3) Final phase.

Therefore, the achievements of the project will be described in the subsequent sections following the same order. To facilitate better insight in planned and achieved results, every section starts with the list of planned activities.

2 Preparing phase

The preparing phase was aimed to define strategy for building Network of Integrated Circuit Design Teaching Centers in Black See Region (NICDTC) and comprises the following actions:

1. Survey of current state at three IC design centers
   - software resources
   - hardware resources
   - human resources
   - IP resources, technologies
   - syllabus
2. SWOT analysis (regarding building a competitive network)
3. Recommendations for required modifications within every center
4. Application for EUROPRACTICE Membership (joining or renewing)

Comprehensive description of all results obtained with the activities listed above is given in the Interim report (34 pages plus three Appendices, 99 pages in total), that is considered as a part of this report.

One meeting was held from 19th to 21st September 2007 in Sozopol Bulgaria during the Electronics'07 Conference. Prof. Marin Hristov from Technical University of Sofia was the host to participants from Faculty of Electronic Engineering, University of Nis, Serbia. Namely, there were Prof. Predrag Petkovic with three Ph. D. students Marko Dimitrijevic, Miljan Nikolic and Borisav Jovanovic. All participants recognized the baseline for the project and agree about the tactics for further activities.

As presented in the Interim report all tasks planned for the Preparing phase of the project were done thoroughly.

3 Executive phase

The executive phase comprised the following activities:

1. Upgrading hardware
2. Updating software
3. Syllabus harmonization
4. Connecting with experienced European Design Centers (Visits, Attending Seminar)
5. Contacting other Design Centers within BSEC region.
6. Mutual Experience exchange (organized within the network)

According to the recommendations accepted during the preparing phase every institution in the network took its part of responsibilities regarding to the activities listed above.

3.1 LEDA Laboratory, Faculty of Electronic Engineering, University of Nis

3.1.1 Upgrading hardware

According to the accepted recommendations for LEDA Laboratory, it was apprised that the present hardware resources are able to cover the current needs for lecturing. However, the needs for hardware in IC Design field are in permanent rise due to the technology development. Therefore it absolutely priority for every node of the network to keep track these development. Unfortunately there are not additional funds available within this project that could cover upgrading hardware in the moment. The best illustration is that five Sun Blade 150 Workstations, that are the hart of our Design Center are no longer orderable from Sun Microsystems. Therefore there are real needs for them to be replaced by Sun Fire V440 Sun 1.593GHz UltraSPARC IIIi that costs approximately $14,000 per item.

Besides there is a need to upgrade 11 PCs dedicated for student training. Besides upgrading motherboards with multicore processors, in the future it will be urgent to invest in replacement of CRT with larger TFT monitors.

TOTAL upgrade costs are appraised to **$ 20,000.**

3.1.2 Updating software

As already presented in the Interim report, the main part of budget was dedicated for software upgrading. Actually, for *Cadence IC Package* with I*C Package option* **$1,550.92** was paid. This discounted price was available through the membership in EUROPRACTICE Service that costs **$1,496.50**.

It is worth to stress that this investment has considerably decreased differences between three design centers, especially between LEDA and ECAD Laboratories.

3.1.3 Syllabus harmonization

The main activities during the Executive phase were assigned to the harmonization of syllabi at Faculty of Electronic Engineering in Nis, that was organized in 3 years for undergraduate and 2 years of master studies (3+2 model) with studies in Armenia and Bulgaria that are organized in 4+1 model.

The complete syllabi of undergraduate and graduate studies were reorganized in 4+1 model and contents of some courses were updated. The new syllabi has been officially accepted by the Faculty council of the Faculty of Electronic Engineering and the Academic council of University of Nis according to serbian law. Afterwards they have been sent for accreditation to the Serbian National Council for High Education. In the moment of writing the report the results have not been known yet.

Table 1 presents the new syllabus for undergraduate studies.

Table 1

No	Title	Semester	Compulsory (C)/ Elective (E)	ECTS	Classes	Exercises	Other
	Common first year						
1	Mathematics 1	1	C	7	3	3	0
2	Electrical Engineering 1	1	C	7	3	3	0
3	Physics	1	C	6	2	2	1
4	Introduction to computer science	1	C	7	2	2	1
5	Society and sustainable development	1	C	3	2	0	0
6	Mathematics 2	2	C	7	3	3	0
7	Algorithms and Programming	2	C	7	3	2	1
8	Electrical Engineering 2	2	C	7	3	2	1
9	Electronic Devices	2	C	6	2	1	1
10	Business Correspodence	2	C	3	2	0	0
	Total for 1st year			**60**	25	18	5
	Second year						
66	Basics Electronics	3	C	6	3	1	1
67	Digital Electronics	3	C	6	2	2	1
68	Signals and Systems	3	C	6	2	1	2
69	Object Oriented Programming	3	C	6	2	1	2
70	Mathematics 3	3	C	6	3	2	1
71	Telecommunications	4	C	6	2	2	1
72	Digital Signal Processing	4	C	6	3	1	1
73	Analog Electronics	4	C	6	2	2	1
74	Object oriented System Design	4	C	6	2	2	1
75	Elective block EMT 1	4	E	6	2	2	1
	Total for 2nd year			**60**	23	16	12
	Third year						
76	English Language 1	5	C	3	2	0	0
77	Computer Networks and Interfaces	5	C	5	2	1	2

78	RF Electronics	5	C	6	2	2	1
79	Multimedial Systems	5	C	6	2	2	1
80	Elective block EMT 2	5	E	5	2	2	1
81	Elective block EMT 3	5	E	5	2	2	1
82	English Language 2	6	C	3	2	0	0
83	Microprocessor Techniques	6	C	6	2	2	1
84	Basics of Power Electronics	6	C	6	2	2	1
85	Elective block EMT 4	6	E	6	2	2	1
86	Elective block EMT 5	6	E	6	2	2	1
96	Practics/Team Project	6	C	3			
	Total for 3th year			**60**	22	17	10
	Forth year						
87	Real Time Systems	7	C	6	2	2	1
88	Power Sources	7	C	6	2	2	1
89	Elective block EMT 6	7	E	6	2	2	1
90	Elective block EMT 7	7	E	6	2	2	1
91	Elective block EMT 8	7	E	6	2	2	1
92	Elective block EMT 9	8	E	6	2	2	1
93	Elective block EMT 10	8	E	5	2	2	1
94	Elective block EMT 11	8	E	5	2	2	1
95	Elective block EMT 12	8	E	5	2	2	1
106	Final exam	8		9			
	Total for 4th year			**60**	18	18	9
	Total			**240**	**88**	**69**	**36**

Table 2 presents subject distribution within the semesters for the **masters** study program ELECTRONICS AND MICROPROCESSOR TECHNIQUES (fifth year of study).

Table 2

No	Title	Semester	Compulsory (C)/ Elective (E)	ECTS	Classes	Exercises	Study work
1.	System on chip	1	C	4	2	1	
2.	Microsensors and microsystems	1	C	4	2	1	
3.	Research and study work	1		7			10
	Module ELECTRONIC COMPONENTS AND MICROSYSTEMS (EKM)						
4.	Elective block EKM 1	1	E	12	6		
5.	Elective block EKM 2	2	E	8	4		
	Module ELECTRONICS AND MICROPROCESSOR TECHNIQUE (EMT)						
6.	Elective block EMT 1	1	E	4	2		
7.	Elective block EMT 2	1	E	4	2		
8.	Elective block EMT 3	1	E	4	2		
9.	Elective block EMT 4	2	E	4	2		
10.	Elective block EMT 5	2	E	4	2		

11.	Research and study work	2		7			10
12.	Diploma work		C	18			
	Total			60	14	2	20

Table 3 presents extraction of one possibility for **System on Chip** specialty on **masters** study program ELECTRONICS AND MICROPROCESSOR TECHNIQUES.

Table 3

No	Title	Semester	Compulsory (C)/ Elective (E)	ECTS	Classes	Exercises	Study work
1..	System on chip	1	C	4	2	1	
2.	Microsensors and mikrosystems	1	C	4	2	1	
3.	Mixed signal circuits design	1	E	4	2		
4	Design of RF integrated circuits	1	E	4	2		
5.	Intelligent machines	1	E	4	2		
6.	Research and study work	1	C	7			10
7.	Simulation and optimization of electronic circuits	2	E	4	2		
8.	Modeling of electronic circuits and systems	2	E	4	2		
9.	Research and study work	2	E	7			10
10.	Diploma work	2	C	18			
	Total			60	14	2	20

3.1.4 Connecting with experienced European design centers

Professors from the Faculty of Electronic Engineering in Nis have visited experienced European design centers in order to establish a closer collaboration in the filed of integrated circuit design education. Although these visits were funded from other sources, their main objective was to introduce the European standards to the education and harmonize the IC design methodology between the design centers in the Black Sea region and EU centers. With some of them there is collaboration within common international projects.

The following centers were visited:

- Electronics and Computer Science, Electronics Systems Design Group, University of Southampton (United Kingdom),
- Electronics Engineering Department, Polytechnical University of Madrid (Espana)

- Faculty of Computer Science and Automation, Dept. System and Control Theory, Technical University of Ilmenau (Germany),

3.1.5 Contacts with other design centers within BSEC region

LEDA laboratory has had very successful cooperation with other neighbor design centers. Naturally, the cooperation is stronger with colleges from former Yugoslavia's republics like Prof. B. Dokic, University of Banja Luka, Bosnia and Hercegovina; Prof. Lj Zivanov, University of Novi Sad, Serbia and Prof. A. Grnarov, SEE University of Tetovo, Republic Of Macedonia. Besides, there are contacts with other countries in BSEC region like with Prof. D. F. Chiper, University of Iasi, Romania and Prof. T. Stouraitis, University of Patras, Greece .

3.1.6 Mutual Experience exchange (organized within the network)

This task was mainly done through e-mail message exchange. However due to the physical proximity of Sofia and Niš, colleagues from Sofia and Niš had opportunity to visit each other. The first visit has been made in September 2007 after first meeting in Sozopol, while the second

3.2 State Engineering University of Armenia (SEUA), Microelectronic Circuits and Systems Interdepartmental Chair

3.2.1 Upgrading hardware

SEUA "Microelectronic Circuits and Systems" Interdepartmental Chair has 5 classrooms with 125 computers. Most of those computers were of 2001. And only a small part of them has been upgraded so far. That is why the mentioned computers were morally old. Particularly, majority of EDA tools was impossible to operate on slow computers.

That is why:

- Server of SEUA "Microelectronic Circuits and Systems" Interdepartmental Chair network which was previously Pentium III (2x1.0GHz) Processor, RAM 256MB, 20GB, 40GB, 2x80GB 7,200 rpm Hard Drive) server was substituted with the new ML150 G3 Non-Hot Plug SATA Server, HP ProLiant ML150G3 Non-Hot Plug SATA Server, 2x Dual Core Intel® Xeon® 5110 (1.60GHz, 1066 FSB) Processor, HP 4GB Fully Buffered DIMM PC2-5300 4X1GB Memory, Embedded 6 Port SATA Controller (does not support factory integrated RAID), 4x HP 250GB SATA 1.5Gb 7,200 rpm Hard Drive, HP 48X CD-ROM, HP NC7781 Gigabit Server Adapter (embedded) 10/100/1000 (Wake on LAN) server.
- Computers of classrooms have been fully updated, 41 Pentium III were substituted with Pentium IV, 10 Pentium IV (1.7GHz) were substituted with higher speed Pentium IV (2.8GHz).

Upgrade has been realized by expenses of Synopsys Armenia CJSC.

TOTAL upgrade costs are appraised to $ 25,600.

3.2.2 Updating software

SEUA "Microelectronic Circuits and Systems" Interdepartmental Chair uses university package of Synopsys EDA tools donated to the Chair in the framework of Synopsys University Programs. Previously the number of licenses was 50, now it is increased to 70. Licenses are periodically updated. The tools are actively used for laboratory works, course projects, diploma works, Master theses, etc.

3.2.3 Syllabus harmonization

The Bachelor and Master degree syllabus at SEUA "Microelectronic Circuits and Systems" Interdepartmental Chair were updated as a result of the analysis of the best practice from the education at the Faculty of Electronic Engineering, University of Nis, Serbia and Faculty of Electronics at Technical University of Sofia. "Digital Integrated Circuit Synthesis and Optimization" and "Scripting Languages" courses have been added. Changes have been made in the structures of several courses ("Digital Integrated Circuits", "Analog Integrated Circuits", "Design for Test"). The new syllabus were reviewed and officially accepted by the Scientific Council of State Engineering University of Armenia. They are now being used in the regular student education.

3.2.4 Connecting with experienced European design centers

Professors from the SEUA "Microelectronic Circuits and Systems" Interdepartmental Chair collaborate with many design centers in the field of integrated circuit design education.

The following centers were among them:

- Moscow Institute of Electronic Technology (Technical University)
- Moscow Engineering-Physics Institute (State University)
- Moscow State Technical University after N.E. Bauman (MSTU)
- San Jose State University (SJSU), California

3.2.5 Contacts with other design centers within BSEC region

Very good contacts were made with Yerevan State University (YSU) represented by the Head of Microelectronics Chair Academician of National Academy of Armenia Vladimir Harutyunyan, American University of Armenia (AUA) represented by the deputy Dean of Engineering College Artak Hambarian, Russian-Armenian (Slavonic) State University represented by the Dean of Microelectronics Faculty Stepan Petrosyan, Kiev Polytechnic Institute

represented by the Head of Physical and Biomedical Electronics Department Aleksandr Fesechko. Common interests for further collaboration were found.

3.3 ECAD Laboratory, Faculty of Electronics at Technical University of Sofia

3.3.1 Upgrading hardware

A SUN Fire V240 Server was upgraded as follows:

- 1 GB DDR memory Option – BGN 4332.00 (conversion rate on 12 December 2007 – 1 USD = 1.3327 BGN) = **$ 3250.54** – invoice No 0000000136/12.12.2007 by ACT Sofia Ltd.

- Motherboard and 1.06 GHz CPU including Heathsink for SUN Fire V240 – BGN 3588.00 (conversion rate on 10 June 2008 – 1 USD = 1.2597 BGN) = **$ 2848.30** – invoice No 0000000230/10.06.2008 by ACT Sofia Ltd.

TOTAL upgrade: **$ 6098.84**

3.3.2 Updating software

N/A

3.3.3 Syllabus harmonization

The Bachelor and Master degree syllabuses at the Faculty of Electronic Technologies, the Technical University of Sofia, Bulgaria were updated as a result of the analysis of the best practice from the education at the Faculty of Electronic Engineering, University of Nis, Serbia and the State Engineering University of Armenia, "Microelectronic Circuits and Systems" Interdepartmental Chair of Yerevan, Armenia. The new syllabus were reviewed and officially accepted by the Faculty council of the Faculty of Electronic Technologies and the Academic council of TU-Sofia in accordance with Bulgarian law and TU-Sofia's internal regulations. They are now being used in the regular student education.

3.3.4 Connecting with experienced European design centers

Leading teachers from the Faculty of Electronic Technologies have visited experienced European design centers for establishing a closer collaboration in

the filed of integrated circuit design education. Those visits had been funded by other projects, but the main objective was to introduce the European standards to the education and harmonize the IC design methodology between the design centers in the Black Sea region and EU centers. The following centers were visited:

- Institute of Electron Technology, Warsaw, Poland;
- University of Aarhus iNano center, Aarhus, Denmark;
- Visit to IDEON Science Park, Lund, Sweden;
- The Nanometer Structure Consortium at Lund University, Sweden;
- University of Copenhagen Nanoscience Centre, Denmark;
- Centre Suisse d'Electronique et de Microtechnique, Neuchatel, Switzerland;
- LETI/MINATEC, Grenoble, France.

3.3.5 Contacts with other design centers within BSEC region

The National Institute for Research and Development in Microtechnologies, Bucharest, Romania represented by the director Prof. Dan Dascalu and KOÇ University, Department of Electrical Engineering, Istanbul, Turkey represented by research engineer Sven Holmstrom were contacted. Common interests for further collaboration were found.

3.4 Summarized achivements of the Network

3.4.1 Updating hardware

These activities were performed by every institution individually. This project helped to articulate needs for hardware upgrading. Unfortunately there were no funds allocated for this purpose and hence achievements in this domain are out of scope of this report.

3.4.2 Updating software

Every institution considered and worked on software design tools updating individually. At the beginning of the project LEDA laboratory had a lag in comparison with other participants. Therefore they assigned major part of the budget from this project in this activity.

Figure 1 illustrates how this project affected closure to the NICDTC goals in domain of software resources coordination.

Figure 1.a presents status before BSEC project started, and Figure 1.b presents the current status in software resources in three institutions.

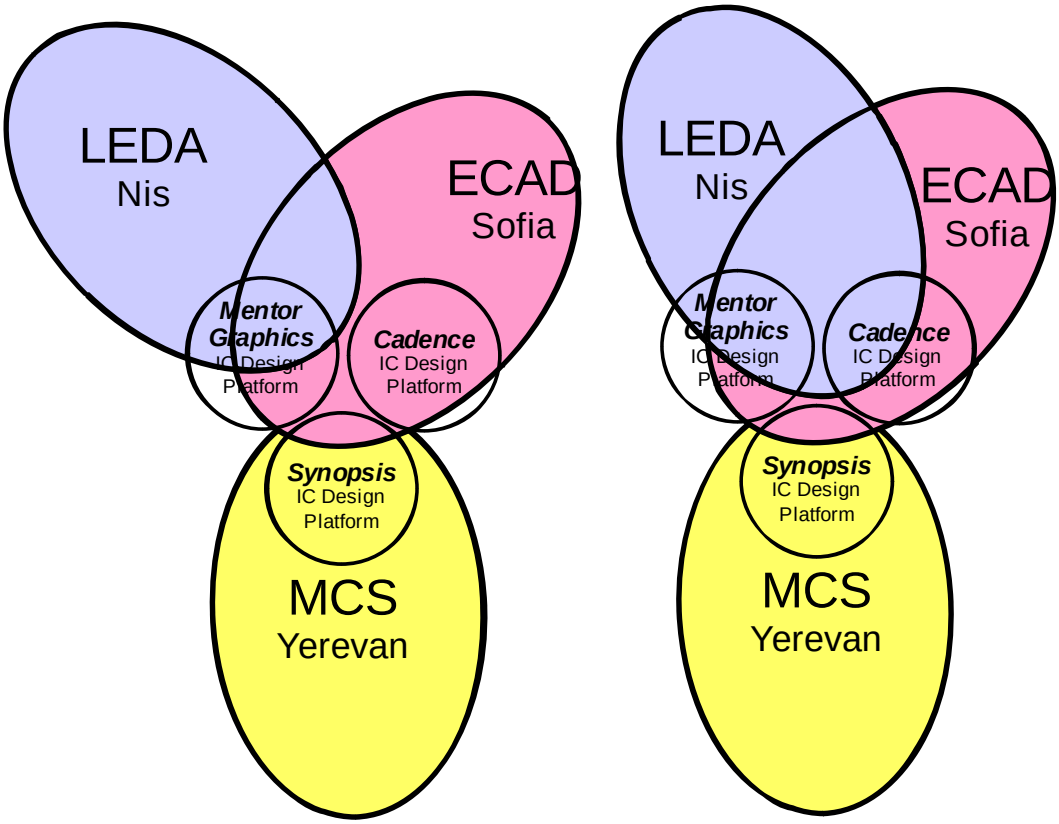

Figure 1

It is important to note that Armenian partner MCS Yerevan is official representative of Synopsis and consequently they relay entirely on *Synopsis´* IC design platform.

Besides, as noted in the Interim report, the cooperation between Design Centers depends more on data format than on tools. Therefore, as far as we are able to interchange data (VHDL description, GDSII files, etc) our collaboration is not jeopardized.

3.4.3 Syllabus harmonization

Syllabus harmonization was one of the most important goals of this project.

At the beginning of the project the major discrepancies were between syllabi at Faculty of Electronic Engineering in Nis, and other two participants because they had quite different structure. Therefore the first task was to transform 3+2 model of studies to 4+1 and that was done as described in subsection 3.1.3.

Besides, all three institutions worked hard to update course content according to the conclusions proposed in the preparing phase and presented in the Interim report.

Eventually after all activities related to syllabi harmonization we have similarity in knowledge and skills that students get in each institution.

Namely knowledge aspect can be viewed as general knowledge and knowledge of IC design field.

In general, during the undergraduate studies students have got similar level of:

- Mathematics
- Electrical Engineering
- Electronic circuits (digital/analog/mixed signal)
- Circuit design
- System design
- Embedded Systems
- Sustainable Design

Moreover, regarding IC Design all three institutions taught

- CMOS process
- ASIC Design
    - Full Custom Design (Transistor sizing)
    - Semicustom Design (Standard Cells)
- FPGA design
- Electronic Circuit Testing
- Basics of Layout

Harmonization in course contents provided students common skills in practical use of the following tools:

- SPICE
- VHDL
- VHDL-AMS
- MATLAB

The more differences are in using different IC design platforms (Mentor Graphics/Cadence/Synopsis platforms) but within every of them students got skills in using

- Schematics editor
- Layout editor
- Verification tools
- Automatic synthesis
- Place and route
- Design rules check
- Electrical rules check

During the graduate studies mainly through different elective courses students can enrich knowledge in

- System on Chip (SoC) design
- Interaction between IC and surrounding circuits
    - (Sensors, Actuators, Equipments, Machines)

- Layout aspects of complex ICs
  - (Mixed Signal IC Design, RF IC Design)
- Advanced theory and tools for IC design
  - (Numerical Analysis, Modeling, Simulation algorithms, Optimization algorithms)

3.4.4 Connections with European Design Centers

As pointed in sections 3.1.4, 3.2.4 and 3.3.4 all participants have had relationships with other European design centers. Summarizing all lists one gets

- Electronics and Computer Science, Electronics Systems Design Group, University of Southampton (United Kingdom),
- Electronics Engineering Department, Polytechnical University of Madrid (Espana)
- Faculty of Computer Science and Automation, Dept. Szstem and Control Theory, Technical University of Ilmenau (Germany),
- San Jose State University (SJSU), California;
- Institute of Electron Technology, Warsaw, Poland;
- University of Aarhus iNano center, Aarhus, Denmark;
- IDEON Science Park, Lund, Sweden;
- The Nanometer Structure Consortium at Lund University, Sweden;
- University of Copenhagen Nanoscience Centre, Denmark;
- Centre Suisse d'Electronique et de Microtechnique, Neuchatel, Switzerland;
- LETI/MINATEC, Grenoble, France.

Moreover, it is important for the future of the Network to accomplish agreement with **AMI Semiconductor (AMIS)** represented by, Design Center Manager and to sign "Frame Co-operation Agreement" with the aim to enhance education, research and development activities in the field of microelectronics. Contacts in this direction started Prof. Petkovic and Prof. Hristov with AMIS branch in Sofia. As important achievement of this Agreement will be possibility to arrange visits for students to AMIS design center and foundry, student competitions and others.

3.4.5 Contacts with other design centers within BSEC region

All participants have made individual contacts with collegues from BSEC region. As we are relatively small community it offen happened that at leeast two participants have mutual connection with the same third-part design center. The strenght of the Network becomes evident after summarizing all these contacts. Namely they are:

- National Institute for Research and Development in Microtechnologies, Bucharest, Romania represented by the director Prof. Dan Dascalu,
- KOÇ University, Department of Electrical Engineering, Istanbul, Turkey represented by research engineer Sven Holmstrom,
- University of Iasi, Romania, represented by Assoc. Prof. D. F. Chiper,
- University of Patras, Greece represented by Prof. T. Stouraitis,

- SEE University of Tetovo, Republic Of Macedonia; and SEEU Technology Park, represented by Prof. A. Grnarov,
- University of Banja Luka, Bosnia and Hercegovina represented by Prof. B. Dokic,
- University of Novi Sad, Serbia represented by Prof. Lj Zivanov,
- Yerevan State University (YSU) represented by the Head of Microelectronics Chair Academician of National Academy of Armenia Vladimir Harutyunyan,
- American University of Armenia (AUA) represented by the deputy Dean of Engineering College Artak Hambarian,
- Russian-Armenian (Slavonic) State University represented by the Dean of Microelectronics Faculty Stepan Petrosyan,
- Kiev Polytechnic Institute represented by the Head of Physical and Biomedical Electronics Department Aleksandr Fesechko.

3.4.6 Mutual experience and exchange

The possibilities for further dissemination of the results and strengthening of the project cooperation were discussed by the participants from Serbia and Bulgaria at the project meeting on 13 May 2008 in Nis associated with the 26th International conference on Microelectronics. It was decided to prepare a proposal for a new joint European project with core participants from the University of Nis, the State Engineering University of Armenia and the Technical University of Sofia. The new proposal could be for the next TEMPUS project call. The next meeting between participants from Serbia and Armenia was planned for 8-12 June 2008 at Plaic Lake, Serbia during the 52nd ETRAN Conference. Seven participants from LEDA Laboratory took place. Namely Prof. Dr Predrag Petković, Prof Dr Vančo Litovski, Prof. Dr Milunka Damnjanović, Prof. Dr Milun Jevtić and Ph. D students Miljana Sokolović, Marko Dimitrijević, Borisav Jovanović and Dejan Mirković. Although six participants from Armenia were supposed to come, due to objective reasons they could not arrive. However, they confirmed by e-mail to agree with the idea about joint application for the next TEMPUS call.

The luck of founds suppressed the idea to provide student exchange and joined work on final exam thesis. However, we decided to exchange presentations of students' projects and got the better insight into outcome of every syllabus.

Examples of students' projects, in the field of integrated circuit design are shown in Appendix1.

4 Final phase

The final phase had two main activities:

- Application for European projects
- Final Report

During the meeting in Niš (May 13, 2007) participants agree to start working on application for the next TEMPUS project call that is expected for autumn 2008. So far, the main topic and the strategy are defined. The subject of the project will be focused on solving one of problems common for all three institutions and similar, potential nodes in the Network. The aim of that project is to diminish treats described as a part of SWOT analysis in Interim Report. More details will be available after submit the application. The coordinator for that project will be the Technical University of Sofia.

5 Financial Part

PROJECT BUDGET	DESCRIPTION OF UNIT	NUMBER OF UNITS	UNIT RATE (in $)	TOTAL AMOUNT (in $)	TOTAL SPENT (in $)
A. SALARIES OR FEES					
1. Faculty of Electronic Engineering, Nis, Serbia	Salary month	2	100	200.00	**0.00**
2. SEUA "Microelectronic Circuits And Systems" Interdepartmental Chair, Yerevan, Armenia	Salary month	2	100	200.00	**0.00**
3. Faculty of Electronics, TU-Sofia, Sofia, Bulgaria	Salary month	2	100	200.00	**0.00**
4. Faculty of Electronic Engineering, Nis, Serbia	Annual License Fee for Cadence IC Package	1	2280	2,280.00	**1550.92**
5. SEUA "Microelectronic Circuits And Systems" Interdepartmental Chair, Yerevan, Armenia	Annual License Fee for Synopsys tools	50 (donation)	0	0.00	**0.00**
6. Faculty of Electronics, TU-Sofia, Sofia,	SoftMEMS, UNIX based Explorer for				**1140,51**[3]

Bulgaria	CADENCE				
7. Faculty of Electronic Engineering, Nis, Serbia	Annual Fee for EUROPRACTICE	1	1140	1,140.00	**1496.50**
8. SEUA "Microelectronic Circuits And Systems" Interdepartmental Chair, Yerevan, Armenia	Annual Fee for EUROPRACTICE	1	1140	1,140.00	1500.00
9. Faculty of Electronics, TU-Sofia, Sofia, Bulgaria	Annual Fee for EUROPRACTICE	1	1140	1,140.00	**1514.43**[1]
SUBTOTAL [5]				6,300.00	7202.36
B. TRAVEL, ACCOMMODATION AND PER DIEMS					
Travel					
1. Faculty of Electronic Engineering, Nis, Serbia	Return ticket to ...	2	400	800.00	**822.31**
2. SEUA "Microelectronic Circuits And Systems" Interdepartmental Chair, Yerevan, Armenia	Return ticket to ...	3	400	1,200.00	1,350.00
3. Faculty of Electronics, TU-Sofia, Sofia, Bulgaria	Return ticket to Nis	3	400	1,200.00	**75.54**[2]
Accommodation					

1. Faculty of Electronic Engineering, Nis, Serbia	Hotel room per night	100	6	600.00	**402.87**
2. SEUA "Microelectronic Circuits And Systems" Interdepartmental Chair, Yerevan, Armenia	Hotel room per night	100	7	700.00	900.00
3. Faculty of Electronics, TU-Sofia, Sofia, Bulgaria	Hotel room per night	100	7	700.00	**243.02**[2]
Per diems				0.00	738.00
1. Faculty of Electronic Engineering, Nis, Serbia		100	8	800.00	**576.30**
2. SEUA "Microelectronic Circuits And Systems" Interdepartmental Chair, Yerevan, Armenia		100	10	1,000.00	
3. Faculty of Electronics, TU-Sofia, Sofia, Bulgaria		100	10	1,000.00	**334.50**[2]
SUBTOTAL				$8,000.00	5442.544
C. PUBLICATIONS AND CONSUMABLES					
Publications					
1. Faculty of Electronic Engineering, Nis, Serbia	Books	2	90	180.00	0.00

2. SEUA "Microelectronic Circuits And Systems" Interdepartmental Chair, Yerevan, Armenia	Books	4	65	260.00	284.37
3. Faculty of Electronics, TU-Sofia, Sofia, Bulgaria	Books	4	65	260.00	0.00
Consumables					
1. Faculty of Electronic Engineering, Nis, Serbia				0.00	0.00
2. SEUA "Microelectronic Circuits And Systems" Interdepartmental Chair, Yerevan, Armenia				0.00	0.00
3. Faculty of Electronics, TU-Sofia, Sofia, Bulgaria				0.00	0.00
SUBTOTAL				700.00	284.37
D. OTHER EXPENSES					
1.Faculty of Electronic Engineering, Nis, Serbia	Conference Fees			0	**455.82**
	Bank transaction expences,			0	**37.24**
	Institution provision,			0	**403.32**

	Mailing expences	1	110.74	0	**110.74**
2. SEUA "Microelectronic Circuits And Systems" Interdepartmental Chair, Yerevan, Armenia	Conference Fees				**465.00**
3. Faculty of Electronics, TU-Sofia, Sofia, Bulgaria	Conference Fees				**389.45**[2]
SUBTOTAL	[redacted]			0	**1860.09**
TOTAL				$15,000.00	**14789.37**
AMOUNT OF FINANCING REQUESTED FROM THE BSEC				15,000.00	
AMOUNT OF OWN CONTRIBUTION IN CASH OR IN KIND (please specify)[6]				0.00	**2789.09**

DISTRIBUTION OF BUDGET AMONG PARTNERS	**REQUESTED AMOUNT (in $)**	**GRANTED AMOUNT (in $)**	**RECEIVED AMOUNT (in $)**	**SPENT AMOUNT (in $)**	**AMOUNT OF OWN CONTRIBUTION IN CASH**
Faculty of Electronic Engineering, Nis, Serbia	6,000.00 (40%)	4,800.00	3,840.00	**5,856.02***	1,056.02
SEUA "Microelectronic Circuits	4,500.00 (30%)	3,600.00	2,880.00	**5,237.37**	1,637.37

And Systems" Interdepartmental Chair, Yerevan, Armenia					
Faculty of Electronics, TU-Sofia, Sofia, Bulgaria	4,500.00 (30%)	3,600.00	2,880.00	**3,697.45**	97.46
TOTAL PROJECT BUDGET	15,000.00 (100%)	**12,000.00**	**9,600.00**	**14,790.84**	**2,790.84**

Notes:

Copies of invoices are given in Appendix 2, together with the currency rates.

[1] The conversion rates EUR/BGN and USD/BGN on the payment dates are as follows:

1 August 2007 – 1 EUR = 1.95583 BGN, 1 USD = 1.4314 BGN;

8 August 2007 – 1 EUR = 1.95583 BGN, 1 USD = 1.4246 BGN;

2 November 2007 – 1 EUR = 1.95583 BGN, 1 USD = 1.3508 BGN;

[2] The conversion rates EUR/BGN and USD/BGN on the payment dates are as follows:
13 March 2008 – 1 EUR = 1.95583 BGN, 1 USD = 1.2555 BGN;

[3] The conversion rates EUR/BGN and USD/BGN on the payment dates are as follows:
4 February 2008 – 1 EUR = 1.95583 BGN, 1 USD = 1.3189 BGN;

*Additional funds are needed for the trip of Prof. Petković to Istambul in September 2008..

6 Conclusion

All Participants were permanently in contact using e-mail. Besides, there were two meetings - one on the beginning of the project (19th to 21st September 2007 in Sozopol, Bulgaria) and second at the end (13th May 2008 in Niš, Republic of Serbia) while the third meeting has to be canceled and postponed because partners from Armenia were not able to come.

There are possibilities to keep living the idea of Network of Integrated Circuit Design Teaching Centers in Black Sea Region through defining common student projects and final exam theses, organizing student competitions and international student' team projects. These activities would not necessarily need huge budget because they can be organized through internet data exchange. This certainly will be considered as topic for further cooperation in the BSEC region.

The existence of the Network of Integrated Circuit Design Teaching Centers in Black Sea Region strongly depends on three founding sources in three periods of subsistence as given in Table 4

Table 4

Period	Funding source
Premature	BSEC PDF Project
Adolescence	Sponsorships from IC foundries and IC Design Tools providers
Mature	Sustained self-funding

Therefore, all three partners agreed to have joint approach to IC foundries and IC Design Tools providers. Good example is almost signed contract with AMIS, Bulgarian branch.